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Power Factor Corrected Zeta Converter Based Switched Mode Power Supply

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Abstract: Switched Mode Power Supply (SMPS) is an integral part of the computer that converts ac to multiple numbers of suitable dc voltages to impart power to different parts of the PC. It contains a diode bridge rectifier (DBR) with a capacitor filter followed by an isolated dc-dc converter to achieve multiple dc output voltages of different ratings. The uncontrolled charging and discharging of the capacitor result in a highly distorted, high crest factor, periodically dense input current at the single phase ac mains; this violates the limits of international power quality (PQ) standards such as IEC 61000- 3-2. Further, the neutral current in the distribution system increases if these PCs are used in large numbers which creates serious problems like overloading the neutral conductor, noise, de-rating of the transformer, voltage distortion etc. In this paper, a non isolated power factor corrected (PFC) converter is being proposed to be used at the front end to improve the power quality of an SMPS for a PC. The front-end converter is able to reduce the 100-Hz ripple in its output that is being fed to the second stage isolated converter.

Keywords: Switched Mode Power Supply, diode bridge rectifier, power quality, and power factor corrected.

I. INTRODUCTION

Personal computers (PCs) have become a part of our day-to-day activities from business to education to infotainment. Switched Mode Power Supply (SMPS) is an integral part of the computer that converts ac to multiple numbers of suitable dc voltages to impart power to different parts of the PC. It contains a diode bridge rectifier (DBR) with a capacitor filter followed by an isolated dc-dc converter to achieve multiple dc output voltages of different ratings. In a single stage SMPS, ac supply is connected to a DBR whose output is processed by a multi-output PFC isolated dc-dc converter for obtaining dc voltages. The reliability of this single-stage SMPS is good however; the output capacitors used are of very high value to reduce the 100 Hz ripple content. For medium power ratings, two-stage SMPS is a commonly accepted solution in the SMPS market for PCs. The first stage is meant for improving the power quality at the PCC and for providing regulated dc output voltage to the isolated (second) stage. Proposed Zeta converter SMPS provides a continuous output current with a low ripple output voltage along with a high level performance which is highly recommendable for PCs.

II. PFC ZETA CONVERTER BASED SMPS CONFIGURATION

The proposed topology is a PFC Zeta converter based multi output SMPS topology as shown in the figure 1.1. At the input, a DBR with filter is connected to a no isolated Zeta converter. It consists of two inductors Lz1 and Lz2, one intermediate capacitor C1, one high frequency switch S and one diode D.

This PFC converter regulates the output dc voltage and draws a sinusoidal current from the ac mains at unity PF. The isolated converter consists of two equal valued input capacitors, two switches, one high frequency transformer(HFT) and filters.

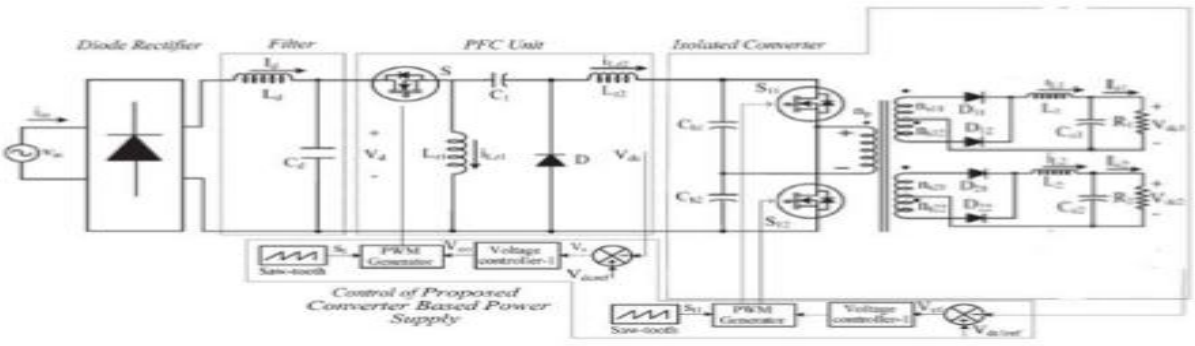

Figure.1.1 PFC Zeta converter based SMPS for PCs

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The filters are used in each output winding to reduce the output voltage and current ripples. Only one of the output voltages is directly sensed and the other output voltages are controlled by the duty cycle of the isolated converter. The winding that is selected for control action is of the largest power rating among all the outputs. Further, to reduce the component stresses, the isolated converter is designed in CCM.

III.ANALYSIS OF OPERATION STAGES OF ZETA PFC CONVERTER

The DCM operation of the output inductor in one switching cycle is shown in Fig. 3.2. The output inductor is designed in DCM and therefore, the current in the output inductor remains zero for a certain time period in one switching cycle .The different modes of conduction in one switching cycle are described as follows. The operational wave form of all three modes as shown in the figure 3.5 Mode I: The PFC switch S turns on; the input voltage supplies energy to inductor Lz1. The intermediate capacitor discharges through the output inductor Lz2. The currents in Lz1 and the output inductor increase linearly.The operation is depicted in fig.1.2

Mode II: The switch S turns off and diode D turns on as shown in Fig.1.3 The stored energy in Lz1 is transferred to the capacitor C1; the output inductor energy is fed to the isolated converter. This stage continues until the current iLz1 equals the negative of the current iLz2.

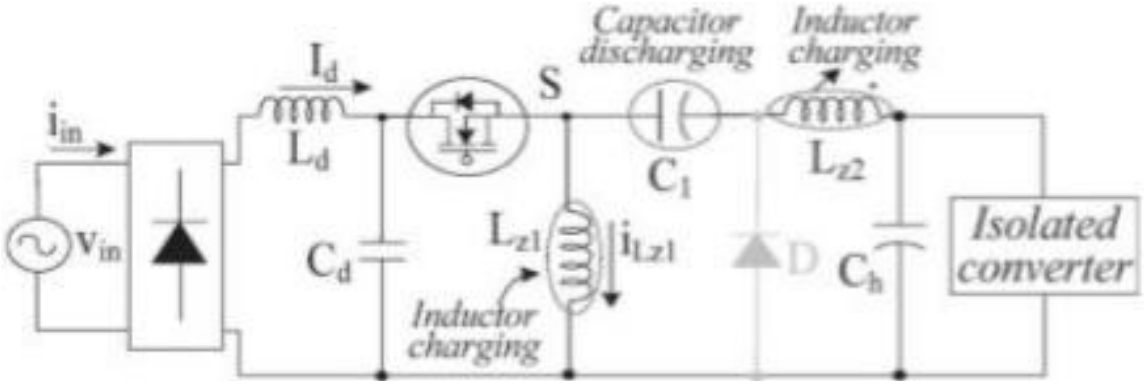

Figure 1.2 Mode 1 Switch ON

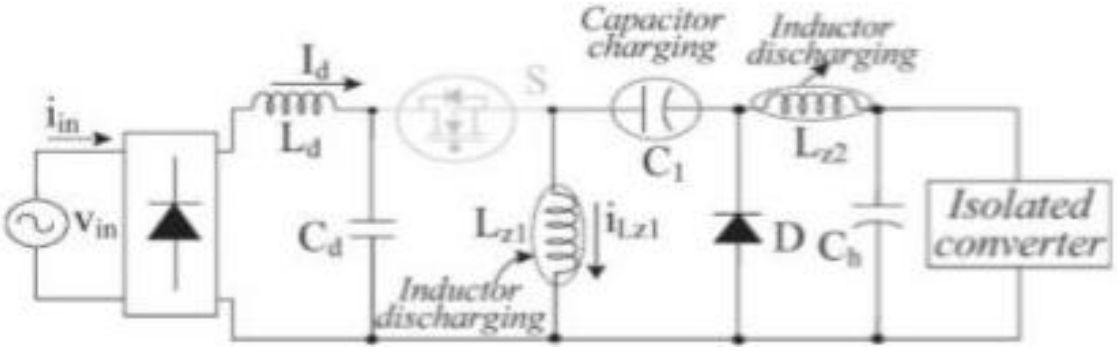

Figure 1.3 Mode 2 Switch OFF

Mode III: The switch and diode both are off in this duration of one switching cycle as shown in Fig.1.4 this state lasts until the start of the next PWM cycle. The output inductor current remains zero in the remaining time ensuring the DCM condition. The operation wave forms as shown in the figure 1.5

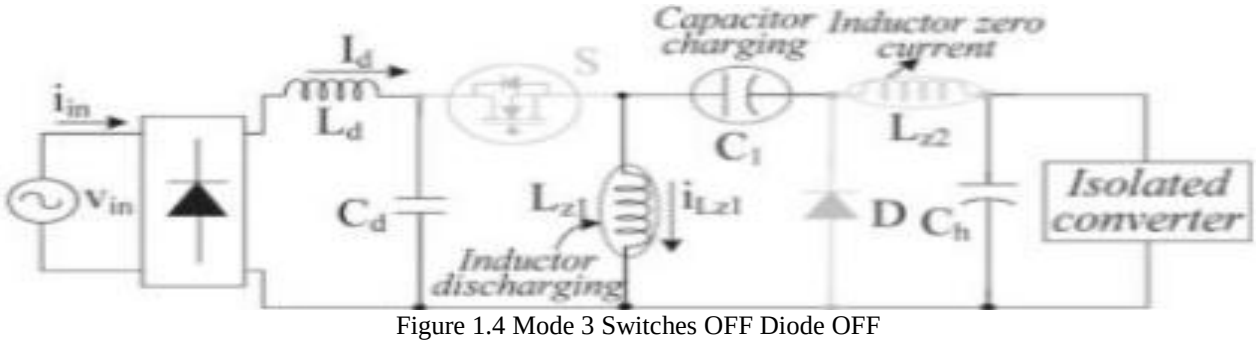

Figure 1.4 Mode 3 Switches OFF Diode OFF

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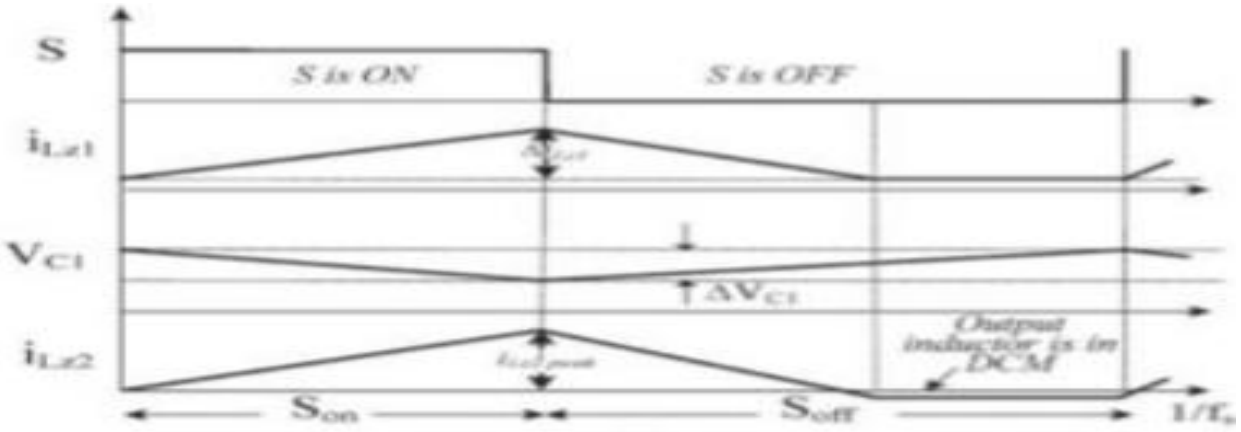

Figure 1.5 Theoretical wave form of zeta converter SMPS

IV. DESIGN CONSIDERATIONS

The design is based on the change in the inductor current during the switch on and off period. The diodes and switches are considered ideal.

The switching frequency considered is high as compared to the line frequency; so, average magnitudes (of currents and voltages) within a PWM period are considered for analysis. The relation between output voltage, V_{dc} and input voltage V_d of the Zeta buck boost converter is expressed as

$$\frac{V_{dc}}{V_d(t)} = \frac{D}{1-D} \qquad (1)$$

Therefore, the instantaneous value of duty ratio, D(t) is expressed as

$$D(t) = \frac{Vdc}{Vin(T) + Vdc} \qquad (2)$$

Input Inductor Selection

$$L_{z1\,min} = \frac{D(t)TV_{in}(t)}{\Delta i_{in}} \qquad (3)$$

$$= \frac{TV_{in}(t)}{\Delta I_{in}} \left[\frac{V_{dc}}{V_d(t) + V_{dc}}\right] \qquad (4)$$

Δis the permitted ripple in the input inductor current and is chosen as 0.5 A.

$$L_{z1\,min} = \frac{220 * 50\mu S}{0.5 * 2A} \left[\frac{220}{198.07 + 220}\right] = 4.55 \qquad (5)$$

Hence a 5mH is selected for CCM operation of the input inductor.

Output Inductor Selection
The critical value of output inductor is estimated as

$$L_{z2\,min} = \frac{(1-D(t))TV_{dc}(t)}{2I_{dc}} = \frac{V_{dc}\,DT}{2I_{in}(t)} \qquad (6)$$

$$= \frac{V_d{}^2 TV_{dc}}{2V_d(t)P_{in}} \left[\frac{V_{dc}}{V_d(t) + V_{dc}}\right]$$

$$= \frac{(198.17\ V)^2 * 50\mu S * 300\ V}{2 * 350W * 198.17\ V} \left[\frac{300\ V}{198.07\ V + 300\ V}\right]$$

$$= 0.08207\mu\ H$$

So the minimum inductance value for operating the output inductor in DCM is estimated as 0.04 μH.

Intermediate Capacitor Selection

$$C_1 = \frac{D(t)TV_{dc}(t)}{2\Delta V_{c_1} R_{dc}} \qquad (7)$$

$$= \frac{50\mu S * 250W}{2\{0.3(200+311.13)\}(220+311.13)}$$

$$= 0.055\ \mu F$$

Δis the permitted ripple in the intermediate capacitor voltage.

The selected value of intermediate capacitor is 0.0667 μF for maintaining it in CCM under all operating conditions.

V. RESULT AND DISCUSSION

The simulation of the power factor corrected zeta converter based switched mode power supply circuit is simulated using corresponding SIMULINK model of the circuit in MATLAB R2010a. Closed loop operation of the circuit is modeled with PI controller and simulated.

The simulation is done for obtaining a dc output voltage, VO=5V and 12v from a sinusoidal input voltage, VIN=220V and frequency = 20 kHz. For validating the working and output waveforms, the converter is simulated with closed loop control by using two control methods. The simulation parameters are shown in following table. For simulating closed loop operation of the converter, the following model is created in Simulink.

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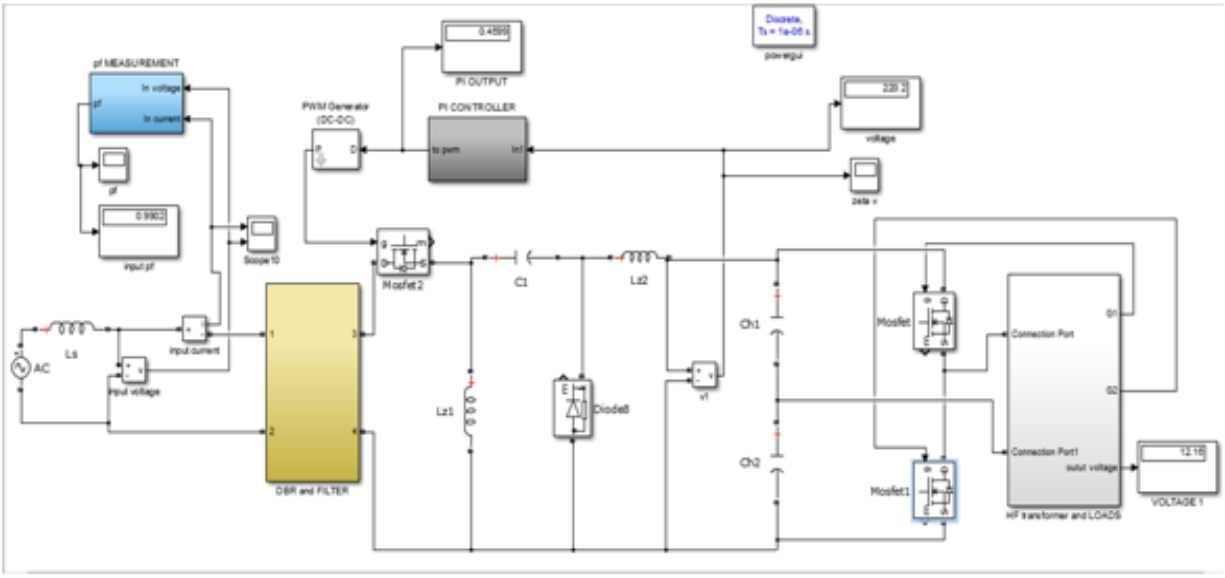

Fig.1.6 MATLAB/Simulink modelby using PI Controller

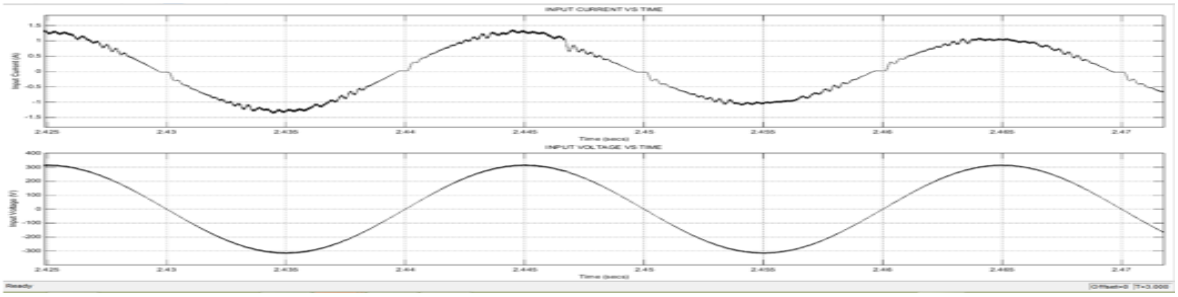

Figure1.7.Waveform Of Input Voltage and Input current

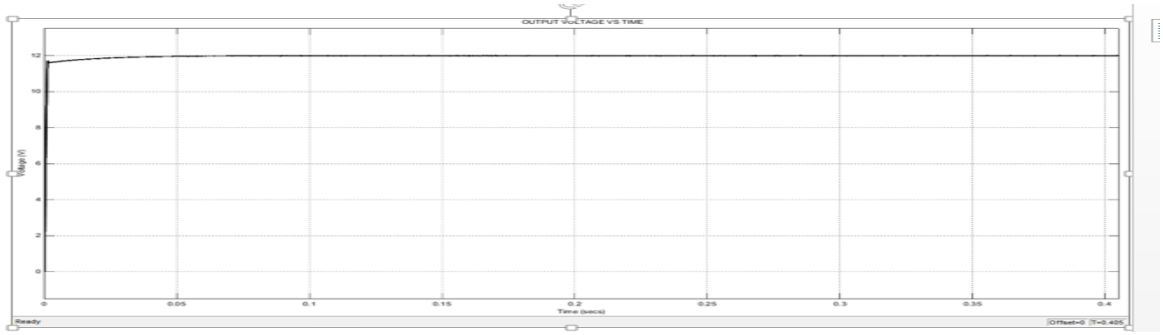

Figure 1.8 Output voltage V_o =12v

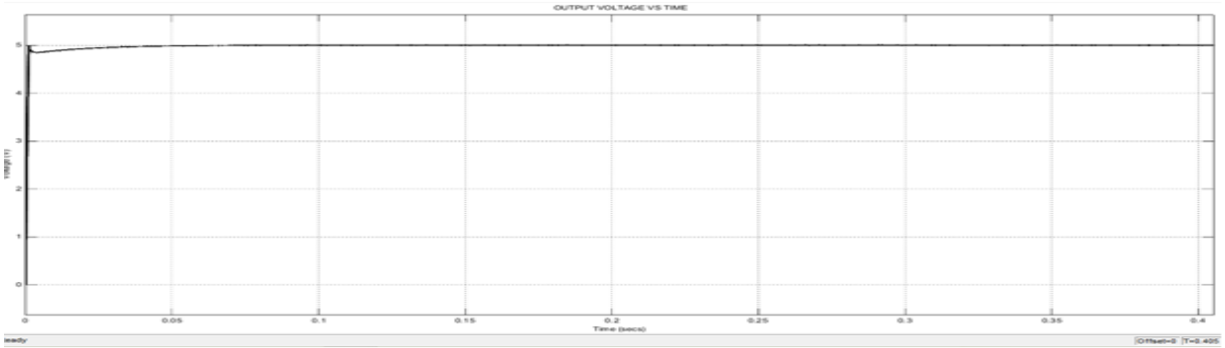

Figure 1.9 Output voltage V_o =5v

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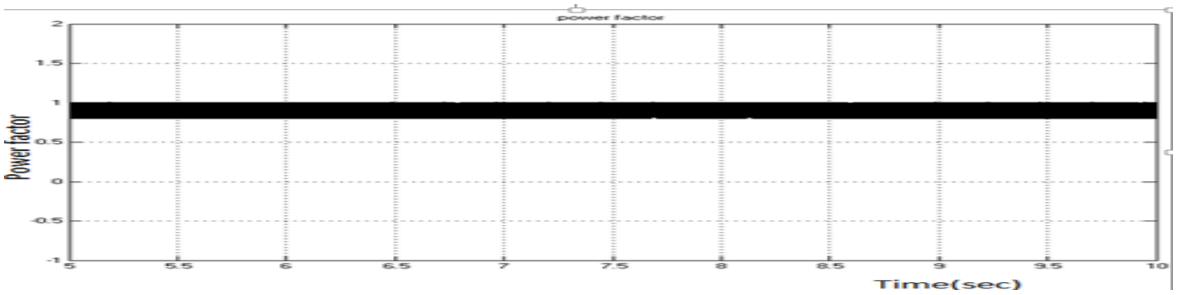

Figure 1.10.Power Factor

VI. CONCLUSION

A DCM operated front-end PFC converter cascaded with a multiple output isolated converter has been used for the design of an SMPS for pcs. It has been designed, modeled, simulated and developed for input power quality improvement and output voltage regulation. All the dc output voltages are regulated by controlling only one output voltage. And one controller is used to regulate the dc bus voltage and for PFC another controller is used to regulate the output voltage. The proposed converter has the advantages over the conventional buck boost converter...

The simulation was done by using PI controller in MATLAB/Simulink. The hardware is implemented using PI controller. Test results obtained from the prototype conform to the ones obtained via simulations. From the recorded test results, it is evident that the proposed power supply is able to mitigate power quality problems that are present in the conventional SMPS systems.

Based on these results, it is concluded that the proposed SMPS configuration in PCs is expected to yield improved THD of ac mains current with almost unity PF under wide range of input voltages and loads.

REFERENCES

[1] Shikha S, B. Singh, G. Bhuvaneswari and VashistBist"Power Factor Corrected Zeta Converter Based Improved Power Quality Switched Mode Power Supply" IEEE transactions on industrial electronics, vol.62, no. 9, september 2015
[2] Limits for Harmonic Current Emissions ,International Electro Technical Standard, Std. 61000-3-2, 2004.
[3] IEEE Recommended Practices and Requirements for Harmonics Control in Electric Power System, IEEE Std. 519, 1992.
[4] H.Aintablian,"The harmonic currents of commercial office buildings due to nonlinear electronic equipment," in Proc. IEEE Conf. SOUTHCON, 1996, pp. 610–615.
[5]] N. Mohan, Power Electronics: A First Course. New York, NY, USA: Wiley, 2011
[6] E.M.GulachenskiandD.P.Symanski,"Distribution circuit power quality considerations for supply to large digital computer loads," IEEE Trans. Power App. Syst., vol. PAS-100, no. 12, pp. 4885–4892, Dec. 1981.
[7] L.Umanand, Power Electronics Essentials& Applications. , India: Wiley India Pvt. Ltd., 2012.
[8] X. Liu, J. Xu, Z. Chen, and N. Wan "Single-inductor dual output buckboost power factor correction converter," IEEE Trans. Ind. Electron., vol. 62, no. 2, pp. 943–952, Feb. 2015.
[9] H. S. Athab, D. D.-C. Lu, A. Yazdani, and B. Wu,"An efficient single switch quasi active PFC converter with continuous input current and low dc bus voltage stress," IEEE Trans. Ind. Electron., vol. 61, no. 4, pp. 1735–1749, Apr. 2014.
[10] H. S. Athab, D. D.-C. Lu, A. Yazdani, and B. Wu,"An efficient single switch quasi active PFC converter with continuous input current and low dc bus voltage stress," IEEE Trans. Ind. Electron., vol. 61, no. 4, pp. 1735–1749, Apr. 2014.
[11] Y.-P. Su et al., "Boundary conduction mode controlled power factor corrector with line voltage recovery and total harmonic distortion improvement techniques," IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3220–3231, Jul. 2014.
[12] Y.-P. Su et al., "Boundary conduction mode controlled power factor corrector with line voltage recovery and total harmonic distortion improvement techniques," IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3220–3231, Jul. 2014.